

REMARKS

Claims 1, 2, 7, 8 and 12 are now pending in this application.

Claim Rejections under 35 U.S.C. § 103

Claims 1, 2, 7, 8 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Plourde, Jr. et al. ("Plourde", U.S. 7,257,308) in view of Dean et al. ("Dean", U.S. 5,303,326).

The Examiner maintains that Plourde, Jr. et al. discloses all the features of independent claims 1 and 7, including ending a recording, but does not specifically disclose moving buffer data after a command to end a recording. Dean has been relied upon by the Examiner as teaching the transfer of audio data after an instruction to end recording, referring to column 12, lines 11-18. The Examiner maintains that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Plourde, Jr. et al. to include the data transfer taught in Dean et al.

The rejections are respectfully traversed.

Independent claim 1 delineates, *inter alia*:

...
in response to the instruction to start recording, the recording unit reserves a dummy area for transfer, after an instruction to end recording, of moving image data and/or audio data that was stored in the memory immediately before the instruction to start recording, and ...

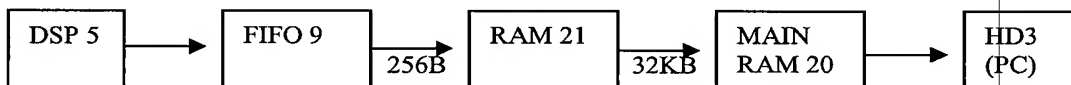
Independent claims 2, 7, 8 and 12 recite similar subject matter.

Neither Dean nor Plourde disclose or suggests that, in response to an instruction to start recording, a dummy area is reserved by the recording unit and after an instruction to end recording, image data and/or audio data that was stored in the memory immediately *before* the instruction to start recording, is moved to this dummy area.

In Column 12, Lines 11-18, Dean discusses:

Data packed by the DSP5 is temporarily stored in FIFO 9 and transferred to RAM 21 by 256 bytes. When RAM 21 (32KB) accumulates data until a 32KB full buffer, the full buffer is once transferred to main RAM 20. When the video recording (audio recording) has been

completed, the data remaining in FIFO 9 is transferred to RAM 21 and is further transferred to main RAM 20 together with the data remaining in RAM 21 (although not a full buffer) (Column 12, Lines 11-18). By the above-transfer, every data processed by DSP has been stored in main RAM 20, and subsequently, the data is stored in HD 3 on PC by a DMA controller at high speed. With this process, high speed transfer can be realized by transferring large quantity of data at one time instead of transferring a small amount of data from DSP to DH little by little over a long period of time.



Therefore, data transferred as described in Column 12, Lines 11-12 of Dean is the last data processed by DSP 5, and *cannot be the data positioned at the first of the contents before a command to start recording is given* as in the present invention.

Neither Plourde nor Dean discloses or suggests that, in response to an instruction to start recording, a dummy area is reserved by the recording unit and after an instruction to end recording, image data and/or audio data ***that was stored in the memory immediately before the instruction to start recording***, is moved to this dummy area. Therefore, claims 1, 2, 7, 8 and 12 are patentable over Plourde and Dean.

CONCLUSION

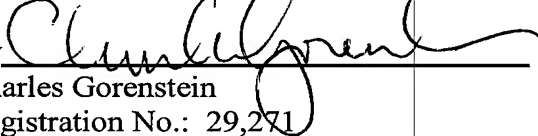
In view of the above, Applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Charu K. Mehta (Reg. No. 62,913) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 022448 for any additional fees required under 37.C.F.R. §§ 1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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